
ASIAN IBIS SUMMIT (TOKYO) AGENDA

Time/Date: Monday, November 16, 2015, 12:30 to 17:30

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Japan Electronics and Information Technology Industries Association (JEITA)
IBIS Open Forum

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ANSYS
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12:30 SIGN IN

13:00 MEETING WELCOME
Shogo FUJIMORI (Fujitsu Advanced Technologies, Chair JEITA IBIS Promotion WG)
Mike LaBONTE (Signal Integrity Software (SiSoft), Chair IBIS Open Forum)

13:10 IBIS Chair's Report
Mike LaBONTE (Signal Integrity Software (SiSoft), USA)

13:25 IBIS Promotion Working Group Report
Shogo FUJIMORI (Fujitsu Advanced Technologies, Japan)

13:40 Introduction to IBIS Version 6.1
Michael MIRMAK (Intel Corporation, USA)
[Presented by Mike LaBONTE (SiSoft, USA)]

13:55 IBIS Simulation for High-Speed Memory Interface Board Suggestions: How to Use IBIS Model Correctly
Masaki KIRINAKA, Akiko TSUKADA
(Fujitsu Interconnect Technologies Limited, Japan)
[Presented by Masaki KIRINAKA
(Fujitsu Interconnect Technologies Limited, Japan)]

14:25 IBIS Interconnect BIRD Update
Walter KATZ (Signal Integrity Software (SiSoft), USA)
[Presented by Mike LaBONTE (SiSoft, USA)]

14:50 BREAK

15:10 Board Design and IBIS Simulation in Consideration of the Delay Control
Makoto MATSUMURO (IB-Electronics, Japan)

15:35 Practical DOE Application in Statistical SI Analysis Using IBIS & How Can We Make IBIS Work Beyond Best Case/Worst Case?
Feng SHI*, Anders EKHOLM**, Zilwan MAHMOD**,
David ZHANG*
(Ericsson, *China, **Sweden)
[Presented by Zilwan MAHMOD (Ericsson, Sweden)]

16:00 IBIS Simulation Case Study: Unexpected Glitch and Using C_fixture
Lance WANG (IO Methodology, USA)

16:25 IBIS-AMI: Concern for PAM4 Simulation
Shinichi MAEDA (KEI Systems, Japan)

16:50 DDR4 SI/PI Analysis Using IBIS5.0
Yumiko SUGAYA (Socionext, Japan)

17:20 CONCLUDING ITEMS

17:30 END OF MEETING
